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APPLICATION NO.		FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,661 07/17/2		07/17/2003	Andrew Harvey Barr	200308575-1	2056
22879	7590	08/22/2005		EXAMINER	
HEWLETT PACKARD COMPANY				NORRIS, JEREMY C	
P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION				ART UNIT	PAPER NUMBER
		O 80527-2400		2841	
				DATE MAILED: 08/22/200	5

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary Examiner								
Jeremy C. Norris The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If the period for reply sepecified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status 1) Responsive to communication(s) filed on 6-13-05. 2a) This action is FINAL. 2b) This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.								
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Disposition of Claims								
proposition of Ordina								
4)⊠ Claim(s) <u>1-34</u> is/are pending in the application.								
4a) Of the above claim(s) is/are withdrawn from consideration.								
S)☐ Claim(s) is/are allowed.								
☑ Claim(s) <u>1-34</u> is/are rejected.								
Claim(s) is/are objected to.								
8) Claim(s) are subject to restriction and/or election requirement.								
Application Papers								
9)☐ The specification is objected to by the Examiner.								
10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.								
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).								
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).								
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.								
Priority under 35 U.S.C. § 119								
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 								
Attachment(s)								
1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)								
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/17/03. Paper No(s)/Mail Date 7/17/03. Paper No(s)/Mail Date 7/17/03. Paper No(s)/Mail Date 7/17/03.								

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DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-28 and 30-34 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,710,258 B2 (Oggioni)

Oggioni discloses, referring primarily to figures 2a&b, a printed circuit board (120) comprising: a conductive layer (210b); a via (145) transecting the conductive layer; and an anti-pad around the via, the anti-pad comprising a pattern of conductive material (220b)having a plurality of voids (see col. 4, lines 40-45) [claim1], wherein the pattern of conductive material is configured to maintain planarity of the printed circuit board (see col. 8, lines 5-10) [claim 2], wherein the pattern of conductive material is configured to prevent settling of dielectric material in the printed circuit board near the via (see col. 8, lines 5-10) [claim 3], wherein the via is configured for data transfer rates greater than approximately 2 GHz (see col. 6, lines 1-5) [claim 4], wherein the pattern of conductive material is configured for data transfer rates through the via greater than approximately 2 GHz (see col. 6, lines 1-5) [claim 5], wherein the pattern of conductive material is substantially circular in shape (see col. 6, lines 5-15) [claim 6], wherein the pattern of

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conductive material is electrically connected to the conductive layer (see col. 6, lines 15-20) [claim 7], wherein the pattern of conductive material is not electrically cormected tù the conductive layer (see col. 6, lines 25-50) [claim 8], wherein the conductive layer comprises a power plane (see col. 7, lines 20-25) [claim 9], wherein the conductive layer comprises a ground plane (see col. 7, lines 20-25) [claim 10], wherein the pattern comprises a symmetric pattern (see col. 6, lines 5-15) [claim 11], wherein the pattern comprises an asymmetric pattern (see col. 6, lines 5-15) [claim 12], wherein the pattern comprises a concentric circles pattern (see col. 6, lines 5-15) [claim 13], wherein the pattern comprises a radial spokes pattern (see figure 2b) [claim 14], wherein the pattern comprises an arbitrary pattern (see col. 6, lines 5-15) [claim 15], wherein the pattern comprises a screen pattern (see col. 6, lines 20-25) [claim 16].

Similarly, Oggioni discloses a printed circuit board comprising: a conductive plane (210b); a via signal barrel (145) transecting the conductive plane; and an anti-pad between the conductive plane and the via signal barrel, the anti-pad having a pattern of conductive material (230b, 235b), wherein a signal can not be transmitted between the conductive plane and the via signal barrel [claim 17], wherein the pattern of conductive material includes a plurality of voids (see col. 4, lines 40-45) [claim 18], wherein the anti-pad is configured to maintain planarity of the printed circuit board (see col. 8, lines 5-10) [claim 19], wherein the anti-pad is configured to minimize stray capacitance between the via and the conductive plane (see col. 6, lines 45-55) [claim 20], wherein the anti-pad is configured to prevent settling of dielectric material in the printed circuit board adjacent the via signal barrel (see col. 8, lines 5-10) [claim 21], wherein the conductive plane

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comprises one of a power plane and a ground plane (see col. 7, lines 20-25) [claim 22], wherein the conductive plane comprises copper (see col. 3, lines 50-55) [claim 23].

Moreover, Oggioni discloses, a method for forming a printed circuit board (120), comprising: forming a conductive plane (210b); forming a via signal barrel (145) transecting the conductive plane; and forming a partially voided anti-pad (230b, 235b) between the conductive plane and the via signal barrel [claim 24], wherein the conductive plane comprises one of a power plane and a ground plane (see col. 7, lines 20-25) [claim 25], wherein the partially voided anti-pad is formed to maintain the planarity of the printed circuit board (see col. 8, lines 1-10) [claim 26], wherein the partially voided anti-pad is formed to minimize stray capacitance between the via and the conductive plane (see col. 6, lines 45-50) [claim 27], wherein the partially voided anti-pad is formed by removing conductive material from the conductive plane in a pattern (see col. 4, lines 40-45) [claim 28], wherein the pattern comprises one of a symmetric pattern and an asymmetric pattern (see col. 6, lines 5-15) [claim 30], wherein the pattern comprises a screen pattern (see col. 6, lines 20-25) [claim 31], wherein the pattern comprises one of an arbitrary pattern and a random pattern (see col. 6, lines 5-15) [claim 32], wherein the anti-pad is substantially circular in shape (see col. 6, lines 5-15) [claim 33], wherein the via signal barrel is substantially circular in shape (see figure 2b) [claim 34].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

- 1. Determining the scope and contents of the prior art.
- 2. Ascertaining the differences between the prior art and the claims at issue.
- 3. Resolving the level of ordinary skill in the pertinent art.
- 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oggioni in view of US 5,844,146 (Murray).

Oggioni discloses the claimed invention as described above except Oggioni does not specifically state that the removing of conductive material is performed by using an etching process. However, it is well known in the art to use an etching process to remove portions of copper to pattern planes in PCBs as evidenced by Murray (see col.

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9, lines 1-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the copper portions in the invention of Oggioni by etching. The motivation for doing so would have been to use a known process with a high degree of control to avoid unwanted copper removal.

Response to Arguments

Applicant's arguments with respect to claims 1-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

SUPERVISORY PATENT EXAMINER

TECHNOLOGY CENTER 2800